XJDeveloper

Overview

XJDeveloper lets you quickly set up and run JTAG tests and programming routines. An automatically generated connection test combined with tests for non-JTAG devices, such as RAM, will check boards for short-circuit and open-circuit faults. Flash memory and EEPROMs can be programmed as well as JTAG devices such as CPLDs, FPGAs and even the internal flash in processors that have a JTAG debug interface.

Even before you have your hardware, XJDeveloper's test coverage report allows you to easily review how much of the board will be tested.

Key Benefits

- Reduce time spent debugging boards
- Improve your time to market and reduce project risk by early design verification
- Reduce your test development time by reusing tests from prototype/design in manufacturing and field support
- Ongoing time savings by test reuse across projects

Rapid test development

XJDeveloper can help you speed up test development by making suggestions about how to categorise the devices and nets in the circuit. If you have BOM information, it will also suggest which model from the installed libraries should be used for each device.

The libraries contain models for simple passive devices such as resistors, complex ICs such as DDR4 memory and devices that can be described using a truth-table such as buffers and logic gates.

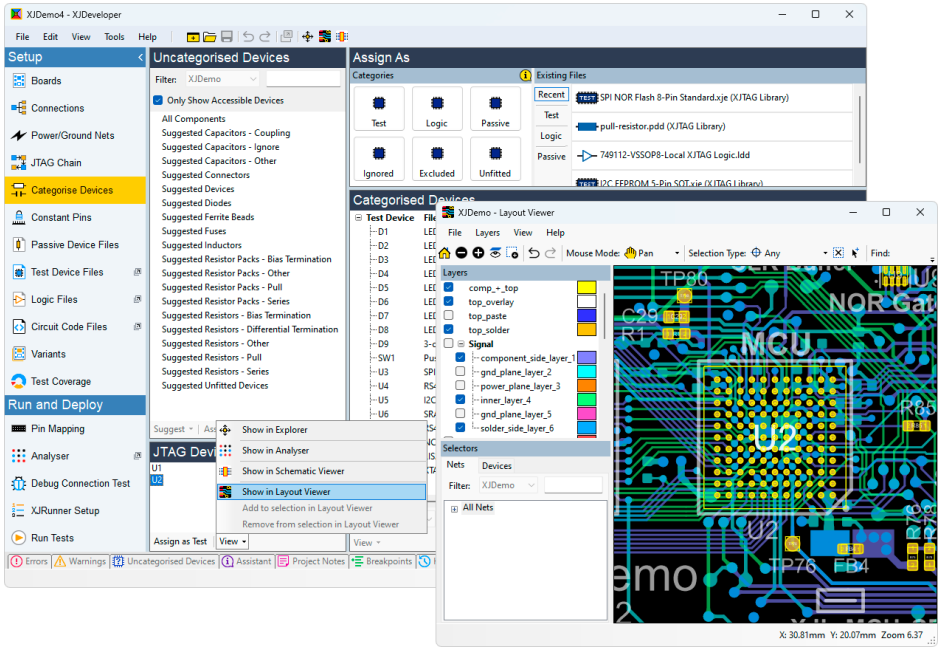
Using these models, a fully functioning test system can be created with no extra programming.

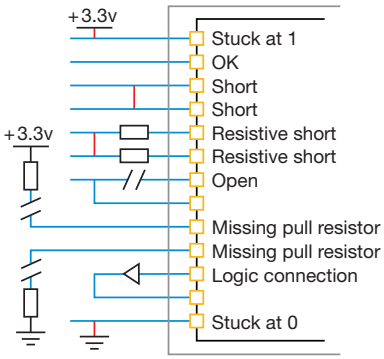
Connection test

XJDeveloper has a built-in connection test for all of the boundary scan enabled pins on your JTAG devices. It checks for a range of short-circuit and open-circuit faults, including shorts to power and ground, resistive shorts and inverted shorts. Pull-up and pull-down resistors are also verified.

As part of its functionality, the connection test also dynamically tests both data and control signals on logic devices such as buffers and logic gates.

When a fault is detected the connection test generates further targeted tests to investigate and pinpoint the location of the error.





Find a wide range of faults using XJDeveloper's connection test

Testing non-JTAG devices

XJDeveloper makes it easy to use devices in your JTAG chain to check the connections to non-JTAG devices. For example, by writing test values to a memory chip and reading them back, you can verify that the data and address lines are free from faults—without booting the processor. Advanced tests, such as sending and receiving Ethernet packets can even test parts of the board with no JTAG access.

Standard data import

XJDeveloper uses netlist information and Boundary Scan Description Language (BSDL) files to understand the JTAG devices and the connections around them. 100+ netlist formats are currently supported. One format, ODB++, also provides layout information that can be used to show the physical location of faults.

XJDeveloper

Powerful testing language

XJDeveloper's high-level programming language, XJEase, provides you with all of the functionality, flexibility and control you require to test the non-JTAG devices in your circuit.

The installed XJEase library contains tests for tens of thousands of devices. You can easily adapt them or write new tests if required, even if you don't have much software experience.

Tests are written in terms of the device being tested so you just need to describe which pins on the non-JTAG device should be driven and which ones should be read. XJEase will work out which part of the JTAG chain needs to be controlled and monitored to implement your requirements.

This not only makes it quicker to develop the tests but also allows you to reuse them for any instance of that type of device in any circuit.

By using high-level language features such as variables, loops, conditional execution, function calls, etc. you can interact with your board in real time, not just "set and check" values.

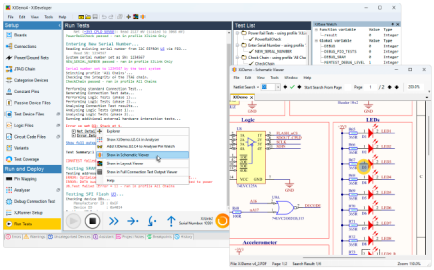
The XJEase debugger features a variable watch window and breakpoints to help get your tests running as quickly as possible.

Integrated Environment

XJDeveloper contains a fully featured debugger, allowing you to step through tests, pause at breakpoints and capture traces of the test while it's running.

The built-in Layout and Schematic Viewers allow you to quickly find any component or net in your circuit, useful when developing your tests or trying to pinpoint a fault. When you have an XJAnalyser license, that is also available inside XJDeveloper.

Once the tests are complete, they can be exported to XJRunner for production.



See the XJRunner, Layout & Schematic Viewer, and XJAnalyser datasheets for more details.

Test coverage analysis

As soon as you have a netlist and schematic, you can create an XJDeveloper project and check the level of test coverage; this is automatically calculated by combining coverage achieved through the connection test and the XJEase testing of non-JTAG devices.

You can download XJTAG's Design For Test (DFT) reference guide that covers many of the issues involved in realising the full potential of boundary scan testing.

Programming flash memory and JTAG devices

The flash memory files in the XJEase library include all of the functionality required to program the flash with an image.

To program many JTAG devices, such as CPLDs and FPGAs, XJDeveloper allows you to run STAPL / JAM or SVF files generated from the device manufacturer's tools.

The internal flash in some processors can also be programmed through the JTAG debug interface.

If your licence includes XJFlash, you can create projects in XJDeveloper which will allow accelerated flash programming, often allowing the process to run at the maximum programming speed of the flash memory, giving further time savings during board production.

Features

- Built-in adaptive connection test
- Automatic logic support
- Library of tens of thousands of standard parts
- Reuse any tests that you write
- Revisions system to handle modified versions of circuits
- Variants to allow multiple build variations on a single PCB design
- Optimises operation of JTAG chains for best performance
- Device programming
  — e.g. CPLDs, FPGAs, flash, processors
- Test coverage analysis before you go to PCB layout
- Integrated Layout & Schematic Viewers
- Advanced testing
  — e.g. Ethernet loopback
- Integration with standard test executives or custom applications
- 100+ netlist formats supported, including ODB++, RINF, Protel, PADS-PCB and ALLEGRO
- Ability to test boards with no netlist
  — just use BSDL files
- Tests 1149.1 and 1149.6 devices

Integration

XJDeveloper tests can be integrated into NI LabVIEW™, Test Stand and ATEasy using the installed examples. Bespoke test executives can also be developed in Python as well as in C#® and Visual Basic® using the .NET interface.

Test development

If all your engineers are busy, XJTAG also offers a consultancy service to create XJDeveloper test systems or bespoke device files to your exact requirements.